REMARKS

The above amendments are submitted in response to the Office Action of September 28, 2000, in the immediate prior application, as discussed with the Examiner at an interview held at the USPTO on April 26, 2001. The Examiner's time and consideration during that interview are greatly appreciated.

Claims Pending:

Claims 36-40 are currently pending and stand rejected. These claims have been clarified regarding certain aspects of the present invention as discussed with the Examiner, to thereby further define over the prior art. Additionally, new Claims 68-76 have been added to more fully claim the present invention, and were also discussed with the Examiner. The claims pending are all directed to methods of reducing voids in metal material that has been deposited into recessed microstructures on the surface of a microelectronic workpiece. The metal is deposited using an electrochemical deposition process, which is specifically recited in Claims 36-40 and 68 as an electrolytic deposition process. Following the deposition of metal to substantially fill sub-micron recessed structures within the surface of a microelectronic workpiece, all claims call for an annealing process under specific conditions.

In particular, Claim 36 calls for electrolytic deposition of metal to substantially fill recessed sub-micron structures on the surface of a microelectronic workpiece, followed by subjecting the surface of the workpiece to an annealing process at a temperature that is at or below about 250° C. Support for this temperature limit is present in the application at page 7, line 19, and at page 27, line 6, referenced herein to show support without limitation of the claims.

Independent Claim 40 as amended corresponds to Claim 36, except that the annealing process is differently recited as occurring at a controlled temperature gradient, which

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temperature decreases along a cross-section in a direction that is toward the surface on which the metal is deposited, as clarified by the above amendment.

New independent Claim 68 calls for electrolytically depositing metal to substantially fill sub-micron recessed structures in the surface of a micro-electronic workpiece that includes at least one low-K dielectric layer. The surface of the workpiece is then subjected to an elevated temperature annealing process, with the temperature selected to be below a predetermined temperature by which the low-K dielectric layer would degrade. Support for this aspect of Claim 68 is provided in the specification on page 7, line 11.

New independent Claim 69 recites a method of electrochemically depositing a metal to substantially fill sub-micron recessed structures in the surface of a microelectronic workpiece, followed by subjecting the surface of the workpiece to an annealing process at a temperature that is at or below about 250 to 300° C. Support for this limitation is found the specification on page 24, line 12.

Finally, new independent Claim 70 corresponds to Claim 69, except that the annealing process is recited as an elevated temperature annealing process that occurs within a chamber, followed by subjecting the workpiece with the deposited metal to a cooling process within the chamber. Support for this aspect of Claim 70 is found in Figures 11-14 and the description of these figures.

Prior Rejections of Claims:

In the outstanding Office Action in the immediate prior application, Claims 36 and 37 were rejected under 35 U.S.C. § 102(b) based on U.S. Patent No. 4,781,801 to Frisby or U.S. Patent No. 5,160,600 to Patel. Claims 36 and 37 were alternately rejected under 35 U.S.C. § 102(e) based on U.S. Patent No. 5,801,444 to Aboelfotoh et al. Lastly, Claims 38-40 were

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rejected under 35 U.S.C. § 103(a) based on Frisby, Patel or Aboelfotoh. Applicants respectfully submit that, as amended, each of the pending claims clearly distinguishes over these references.

A. U.S. Patent No. 4,781,801 to Frisby

Frisby is directed to a method of copper plating gravure rolls, i.e., rolls used in printing processes. Frisby teaches that copper plating applied to gravure cylinders using conventional processes is unsuitable for electronic engraving of gravure rolls. Specifically, Frisby states, "these copper deposits may show the initial requisite hardness value, but within a short period of time, undergo spontaneous structural changes (often referred to as annealing) so that the deposit is too soft for commercially acceptable electronic engraving." Frisby then goes on to describe the invention disclosed therein as using a particular bath composition so as to produce a deposited metal that is not subject to recrystallization, thereby suppressing annealing. Column 4, lines 3-15.

Specific examples are then given where samples are subjected to an accelerated annealing test by heating to 100° C to determine whether undesirable annealing occurs, as in the reference examples, or whether therein annealing was desirably avoided in accordance with the disclosed invention, as set forth in Example 1. Frisby thus teaches explicitly away from annealing in general, including low temperature annealing, stating that it results in undesirable properties. The disclosure of Frisby is thus contrary to the claimed annealing steps in the present application.

Moreover, Frisby is directed to bulk plating of copper onto gravure rolls, in thick layers of approximately 0.005 inches, or approximately 125 μM. See, e.g., column 6, line 31. Thus, even if one is to ignore the disclosure in Frisby that recrystallization of metal through annealing is undesirable, and particularly low temperature annealing is undesirable, the deposition solutions and methods of Frisby are totally inappropriate for use in microelectronic structures;

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microelectronic workpiece metallization is much more carefully controlled, and concerns much thinner and highly uniform deposits and films having specific electrical transmission properties. This distinction has been reflected in each of the claims by recitation of deposition to substantially fill sub-micron recessed structures on a microelectronic workpiece.

In addition to the differing substrates and thicknesses, Frisby does not in any way disclose or suggest depositing metal within a recessed structure of any type, or particularly within a sub-micron recessed structure.

Applicants thus submit that Frisby does not disclose or suggest the present invention, and in fact teaches away from the present invention.

B. U.S. Patent No. 5,160,600 to Patel

Patel discloses a process for electroless plating of decorative coatings onto plastics such as ABS, and more particularly to a process for carrying out blistering tests on such decorative coatings.

Initially it is noted, with respect to Claims 36-40 and 68, that Patel discloses electroless plating solutions, rather than electrolytic plating solutions, and electroless processes rather than electrolytic processes. See, e.g., column 4, lines 8-12 and Example 1. It is only after the electroless layer is laid down that electrolytic copper may be deposited as set forth in Example 1. Electroless and electrolytic solutions are not highly predictable, and must be specially formatted and adapted for these two processes. Thus, Claims 36-40 and 68 define over Patel at least by virtue of this distinction.

More particularly, Patel is not directed to depositing metals on microelectronic workpieces, but rather to depositing decorative coatings onto plastics. Again, the high degree of uniformity, thin thicknesses, electrical transmission properties, and crystalline properties

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required for microelectronic structures are vastly different than those required for a decorative coating deposited onto plastic.

Patel also fails to disclose or suggest in any way deposition of metals into recessed structures, or into recessed microstructures.

Finally, Patel is directed to a method of conducting a blistering test on decorative coatings, not to methods of filling voids. The coating that is deposited is thick, approximately 0.1 to 0.3 inches. (See, e.g., Example 2.) This would be an entirely unsuitable coating thickness for deposition onto microelectronic structures.

It is thus submitted that Patel fails to disclose or suggest several significant aspects of the inventions, including the deposition of metals into recessed microstructures of microelectronic workpieces, and in particular electrolytic deposition processes. Further, there is no disclosure or suggestion of controlling temperature to avoid degradation of a low-K dielectric layer, as set forth in Claim 68.

C. U.S. Patent No. 5,801,444 to Aboelfotoh

Aboelfotoh is directed to forming a copper-silicide or copper-germanide layer, that essentially serves as a barrier layer. Copper is first deposited on the Si or Ge substrate, and then is heated to form the silicide or germanide. See, e.g., abstract. These materials are deposited in very thin layers, as low as 125 angstroms to 5,000 angstroms. See, e.g., column 4, line 16-26.

Perhaps more significantly, Aboelfotoh does not disclose electrochemical or electrolytic deposition of these materials. Rather, reference is made only to depositing these materials by CVD, sputtering or evaporating. See column 6, lines 1-2; column 6, lines 49-52; and column 8, lines 12-14. The applicants submit that Aboelfotoh also fails to disclose or suggest in any way the present claimed invention.

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CONCLUSION

In view of the above, applicants submit that none of the references, alone or in combination, disclose or suggest the present invention. Further, modifying the references to obtain the present invention would be contrary to the disclosure of Frisby, would result in deposited material which is unsuitable for use in microelectronic structures as disclosed in Patel or Aboelfotoh, and would not result in an electrochemically or electrolytically deposited processes, in accordance with Aboelfotoh.

In view of the above, applicants respectfully request reconsideration and passage of the application to issue. Should there be any remaining issues, the Examiner is invited to telephone the undersigned attorney.

Respectfully submitted,

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I hereby certify that this correspondence is being delivered via facsimile to the Commissioner for Patents, Washington, D.C. 20231, Attention: Examiner G. Wyszomierski, facsimile number 703-872-9039 on the below date.

Date: June 13, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE JUNE 13, 2001

In the Claims:

Claims 68-76 have been added.

36. (Amended) A method for reducing voids in a metal material that has been electrolytically deposited into recessed microstructures defined in a surface of a microelectronic workpiece comprising:

[the step of] electrolytically depositing a metal to substantially fill recessed sub-micron structures in the surface of the workpiece; and then

subjecting the workpiece to an annealing process at a temperature that is at or below about 250 degrees Celsius.

40. (Amended) A method for reducing voids in a metal material that has been electrolytically deposited into recessed microstructures defined on a surface of a microelectronic workpiece comprising:

[the step of] electrolytically depositing a metal to substantially fill recessed sub-micron structures on the surface of the workpiece; and then

subjecting the workpiece to an annealing process in which the workpiece is subject to a controlled temperature gradient in which the temperature decreases along a cross-section of the workpiece in a direction that is [opposite to the direction of the formation of the deposited metal material] toward the surface in which the recessed sub-micron structures are formed.

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